66TH IEEE INTERNATIONAL MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS

MWSCAS 2023

Floating Gates are an Ideal Primitive for Analog Neural Networks

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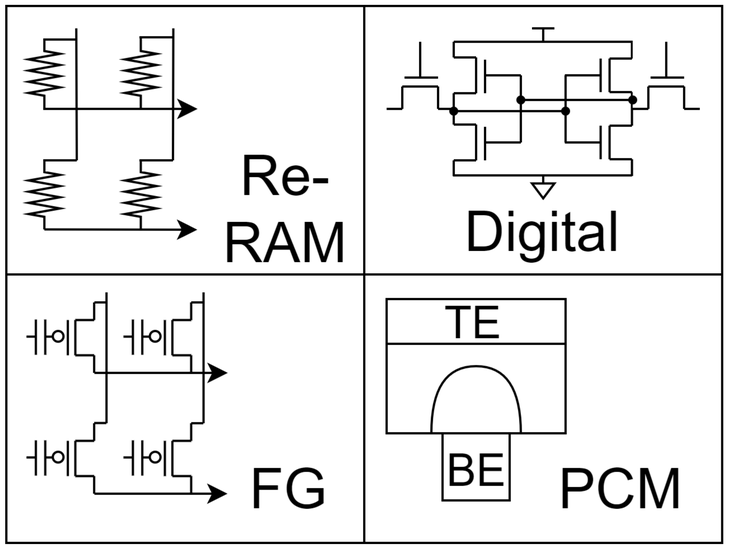
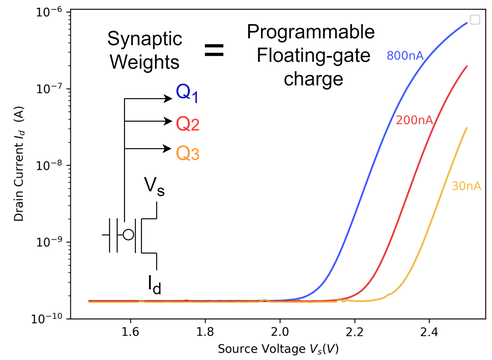
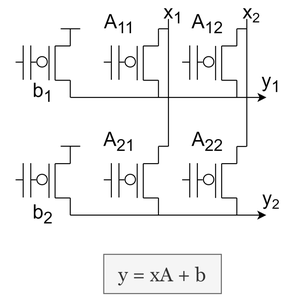


	Precision	Drift ?	Current draw	Fabrication Maturity
ReRAM [1]	~4 – 5 bits	Yes	mA	No
Digital	4/16 bits	No	mA	Yes
Phase Change memory [2]	~ 3 bits	Yes	uA	No
Floating Gates [3]	13 bits	No	pA to nA	Yes

Major Compute-in-Memory (CIM) primitives explored in research currently.

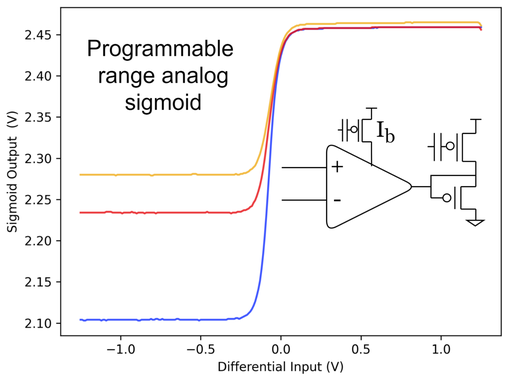
Aside from base properties, the versatility of the FG FET is what sets it apart. Ability to integrate into many more circuits allows it to overcome the CIM data converter bottleneck

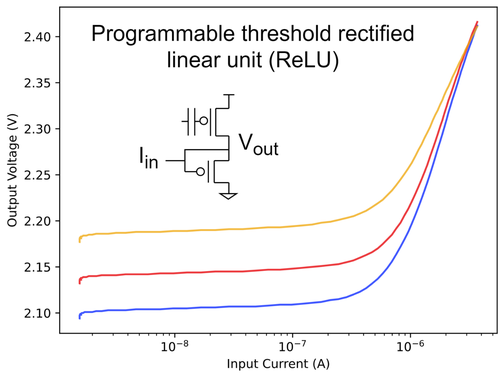




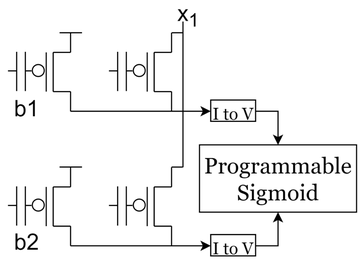
FGs allow for a wide range of programmable currents (pA to uA) with excellent selectivity, ideal for a crossbar.

A significant bottleneck of most CIM structures is dealing with analog information flowing in and out of the crossbar. Data converters are placed at the periphery and burn away efficiency gained.

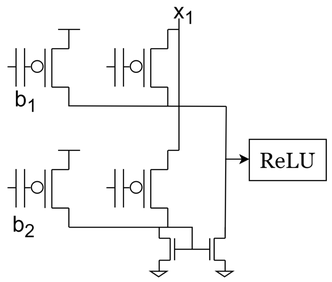




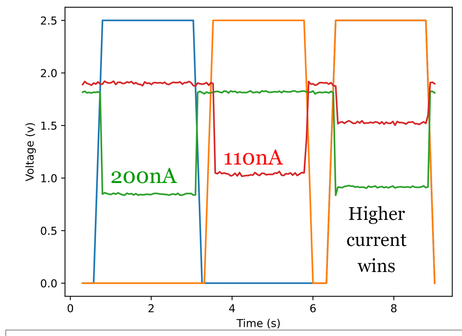
By designing reconfigurable activation functions, that limitation can be surpassed for an efficient, fully analog neural network.

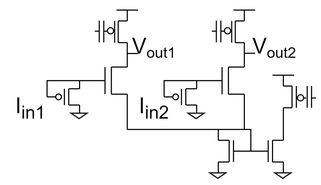


Differential input sigmoid



Differential input ReLU





Winner-Take-All as a Softmax

A WTA as softmax allows for the final stage of a network to be performed in the analog domain, coupled with a simple inverter for digital interfacing.

References:

1. Wan, W., Kubendran, R., Schaefer, C. et al. A compute-in-memory chip based on resistive random-access memory. Nature 608, 504–512 (2022).
2. Manuel Le Gallo and Abu Sebastian 2020 J. Phys. D: Appl. Phys. 53 213002
3. S. Kim, J. Hasler, and S. George, “Integrated floating-gate programming environment for system-level ics,” IEEE Transactions VLSI, vol. 24, no. 6, pp. 2244–2252, 2016.