ASHeS: Analog System High-level Synthesis for Reconfigurable Computing

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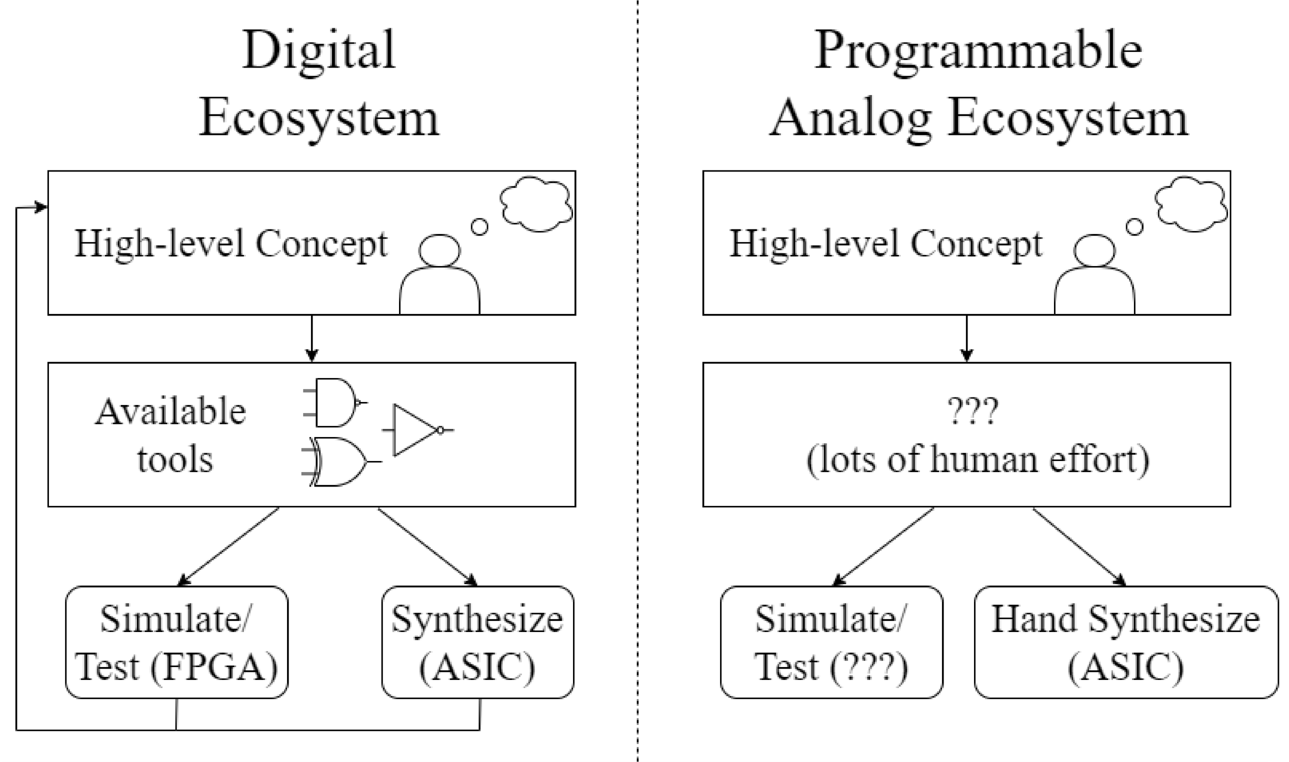
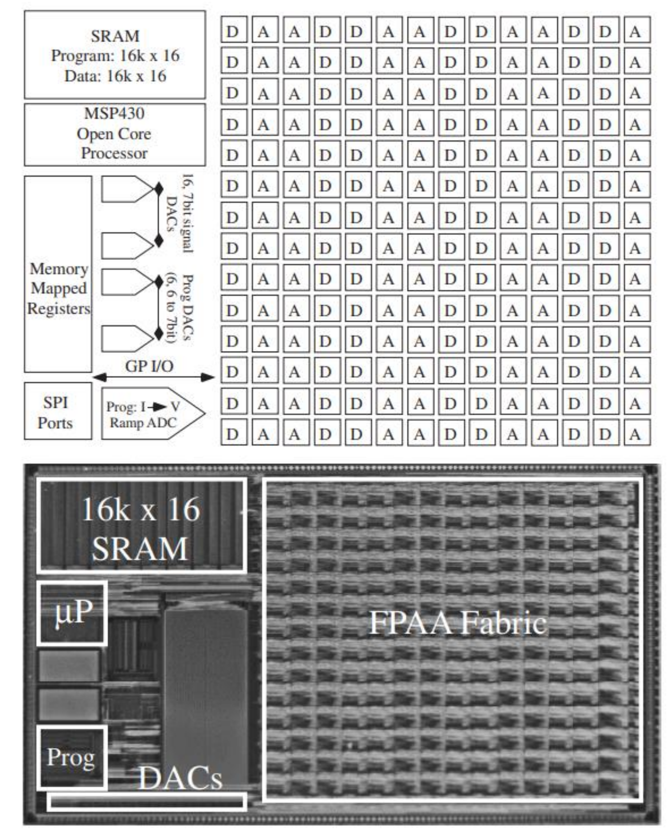
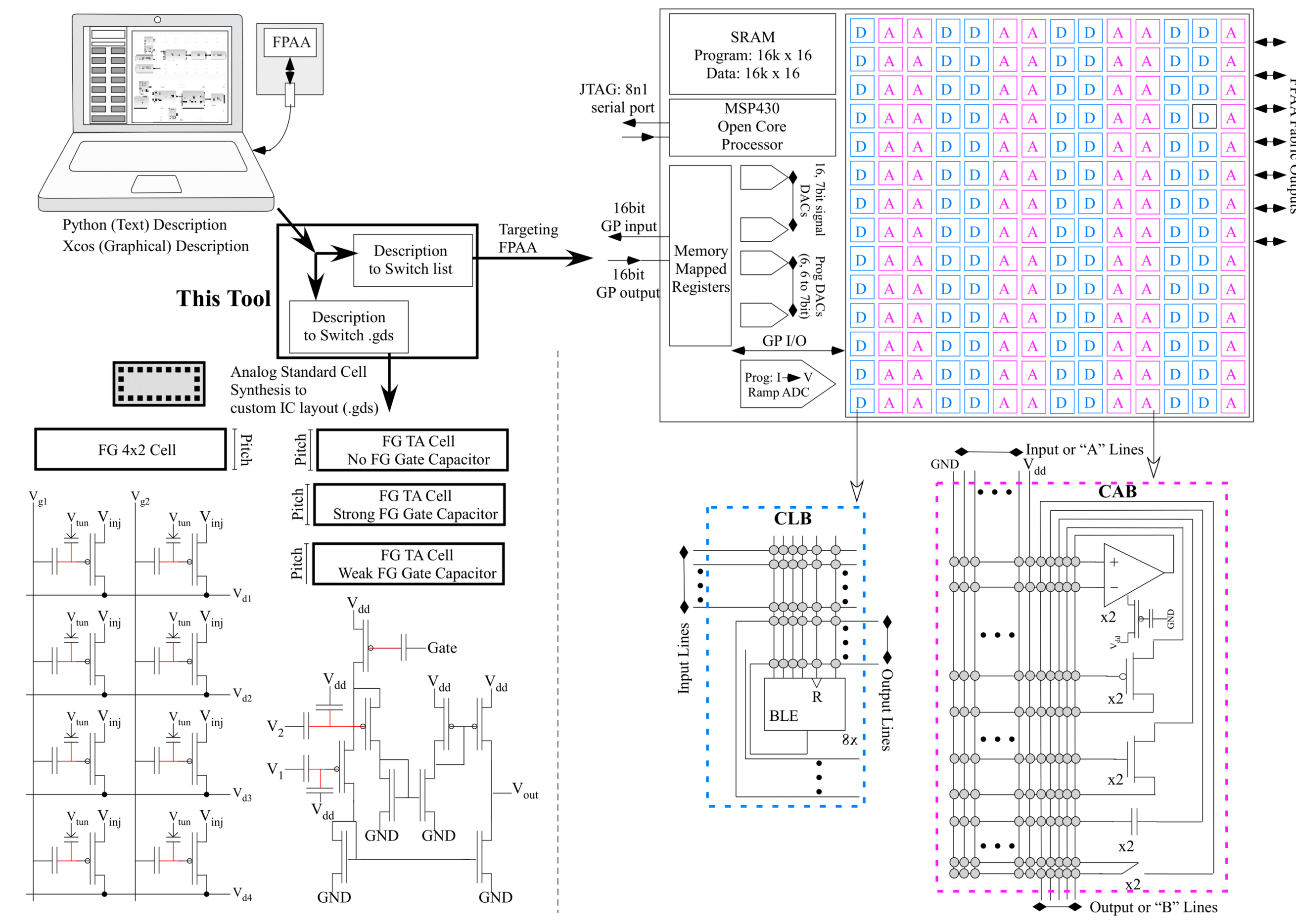
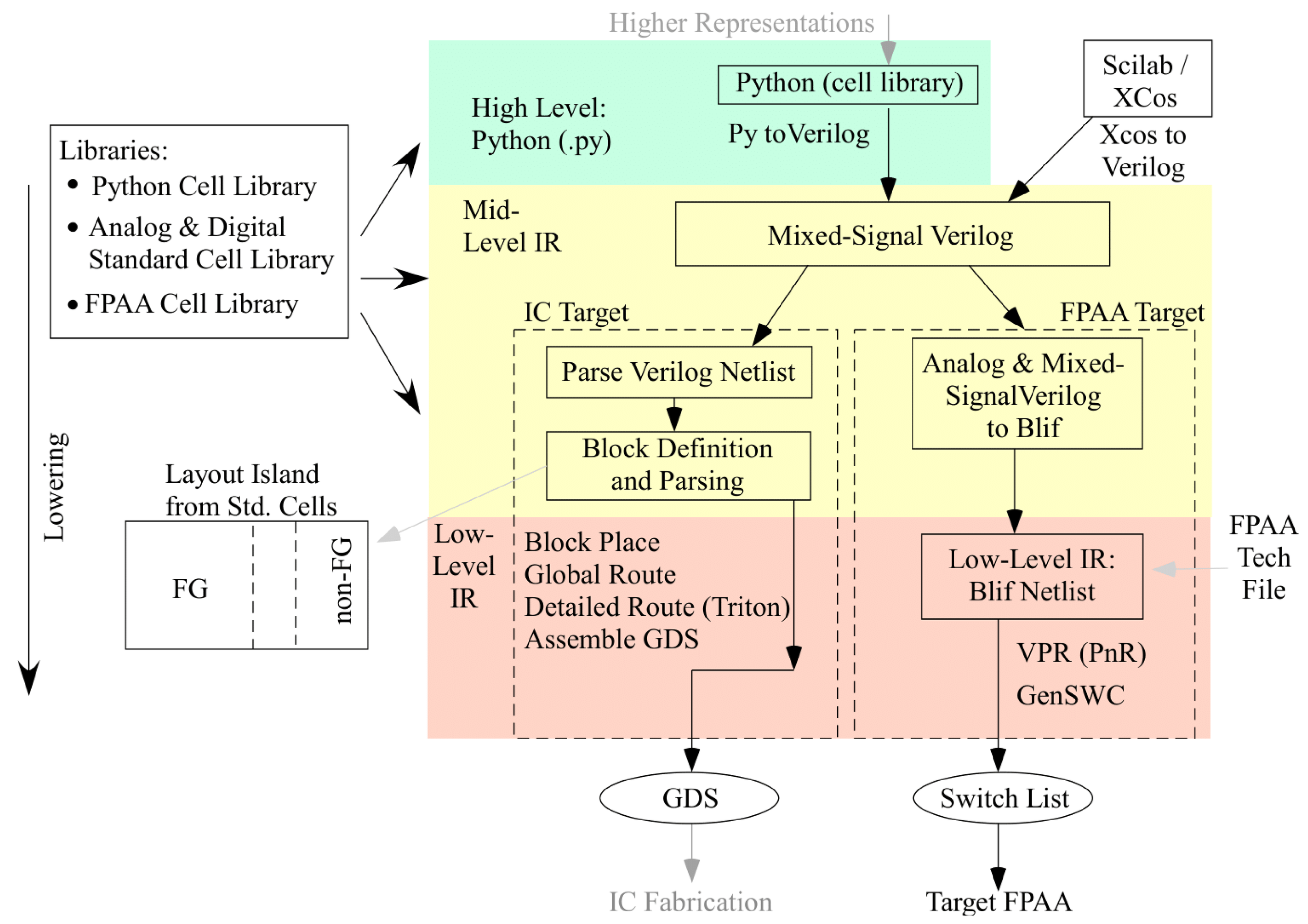


Motivation: There is a lag between digital and analog design tooling, particularly for large scale computing



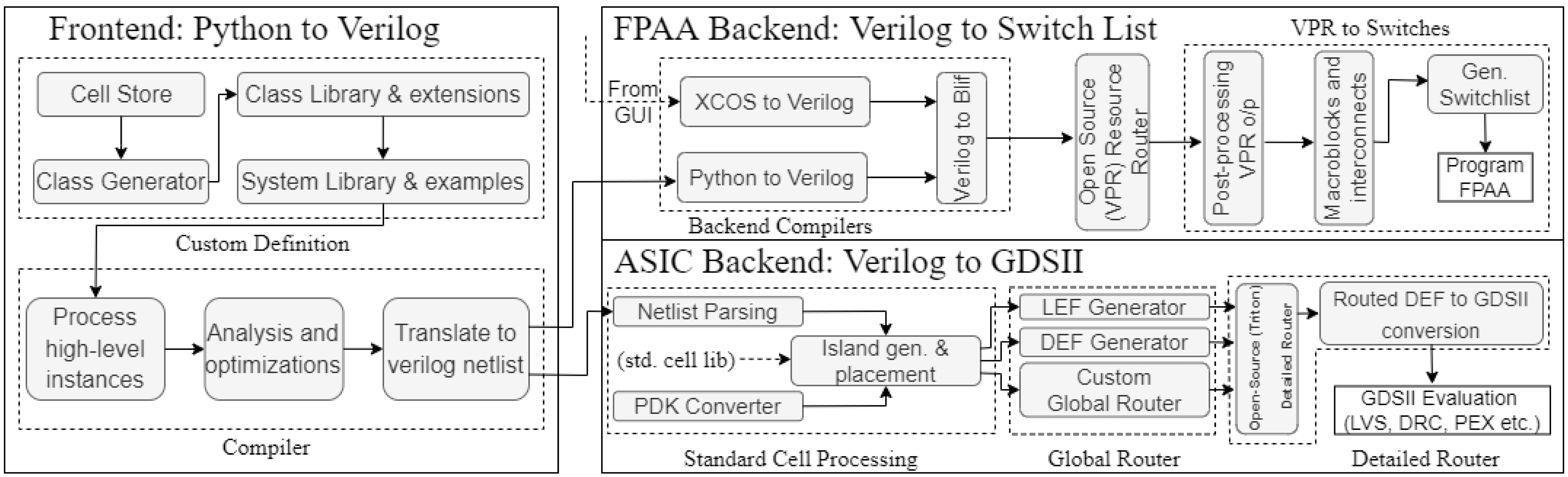
Field Programmable Analog Array (FPAA)

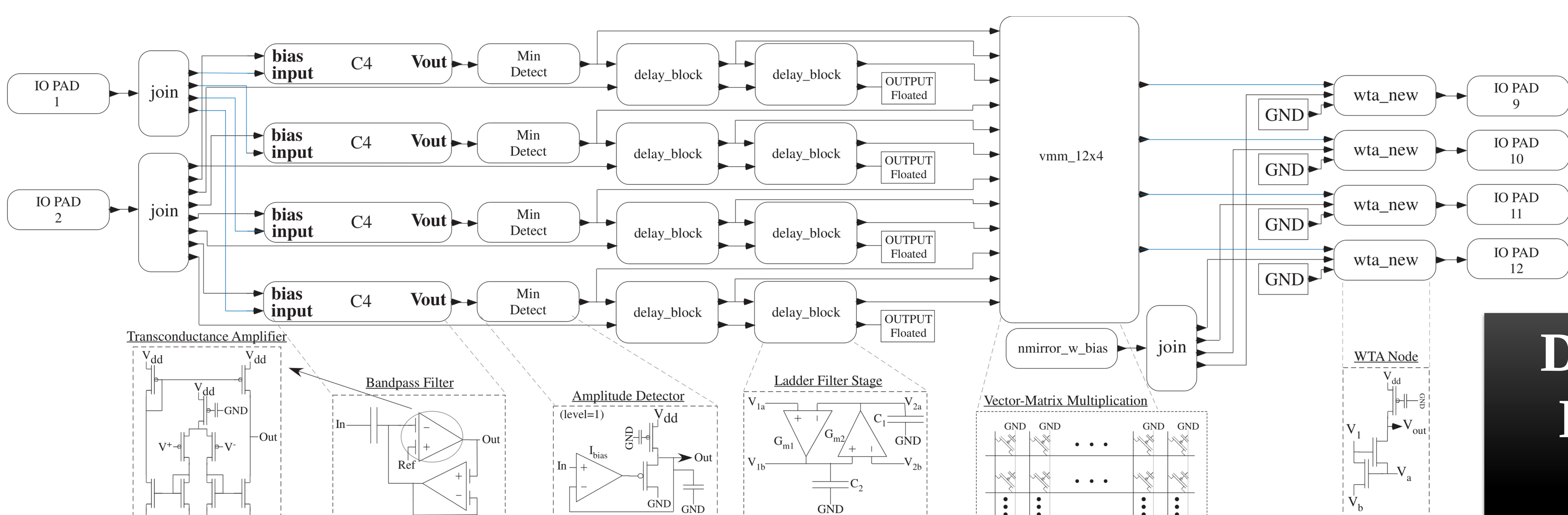




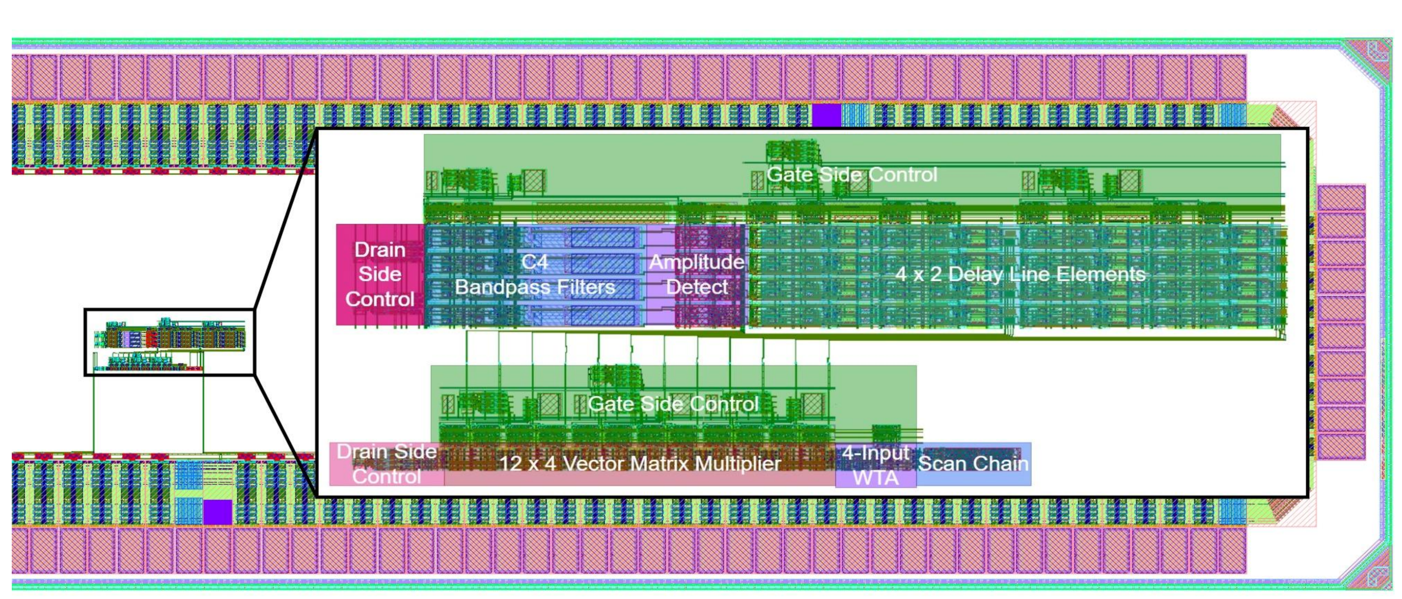
Tool Flow

ASHeS is bifurcated into a frontend, high level definition with a compiler and a backend to synthesize netlists to either programmable switch lists or fabrication-ready GDSII layout files.





Design of an Embedded Speech Recognition System



ASIC synthesis of design

	FPAA	ASIC
Space Utilization	Cab count = 18	Area = 252 um^2
Wire Nets	32	29
Num FGs	537	68
Verilog LoC	89	20

FPAA synthesis of design

Summary

We demonstrate an open-source, end-to-end unified tool flow for automated synthesis from a high-level representation to both a reconfigurable platform and a fabrication ready layout file.